Xyce™ Parallel Electronic Simulator Release Notes

Release 1.1

Scope/Product Definition

The **Xyce**™ Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://www.cs.sandia.gov/xyce.

Hardware/Software Information

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 1.1.

Supported Platforms

Xyce 1.1 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms:

- SGI IRIX 6.5.2 (serial and parallel using SGI MPI 3.3)
- Redhat Linux, version 7.2 on Intel Pentium architectures (serial and parallel using MPICH or LAM MPI)
- Sun Microsystems Solaris 8.0, on UltraSPARC and later architectures (serial)
- Tru64 on HP Alpha (serial and parallel)
- FreeBSD on Intel Pentium architectures (serial and parallel using MPICH or LAM MPI)
- Microsoft Windows (serial)
- Apple OS X (serial)

Build Capability but Not Supported

- CPlant™ on hp Alpha (serial)
- ASCI White (IBM) (parallel)

Hardware Requirements

The following are *estimated* hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*
- 200MB disk space

Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required *to build* **Xyce** on a platform. These are *only* required when building **Xyce** from source. These are:

- **Trilinos** Solver Library (Sandia, http://software.sandia.gov/Trilinos) including the following packages (libepetra.a, libaztecoo.a, libifpack.a, libepetraext_trans.a, libamesos.a, libtriutils.a, liby12m.a, libzoltanCPP.a (parallel only))
- SuperLU (http://www.nersc.org) (libsuperlu.a)

For parallel builds, the following are additionally required:

- MPI (http://www-unix.mcs.anl.gov/mpi/) library for message passing (version 1.1 or higher), such as MPICH or LAM
- **Zoltan** (Sandia, http://www.cs.sandia.gov/Zoltan) and its associated libraries (libzoltan.a, libparmetis.a, libmetis.a)
- **Chaco** (Sandia, http://www.cs.sandia.gov/CRF/chaco) (libchaco.a, libChacoCPP.a (Xyce-version))
- libblas.a, liblaspack.a
- Gnome XML C library libxml2.a
- CoMeT Data Management library (libCDM.a)

Xyce™ Release 1.1 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. As this is the initial Version 1.1 release, some of this documentation is in "Draft" mode and is incomplete.

- **Xyce**™ User's Guide, Version 1.1
- **Xyce**™ Release Notes, Version 1.1
- **Xyce**™ Theory Document
- High Performance Electrical Modeling and Simulation Software Normal Environment Verification and Validation Plan, Version 1.0
- High Performance Electrical Modeling and Simulation Software Normal Environment Verification and Validation Plan Self Assessment, Version 1.0
- **Xyce**™ Test Plan

New Features and Enhancements

Highlights

This release is the first full release following the Version 1.0 release. It encompasses many key bug fixes as well as key robustness and performance enhancements. Furthermore, many features that we previously provided as options have now been thoroughly tested and are now defaults (e.g., direct-matrix access for improved performance). Lastly, several new features continue to move **Xyce** towards a more full-featured circuit simulation tool. Highlights for this release are:

- Improved performance (approximately 30% improvement) of the sparse-direct linear solver (KSparse) for serial calculations.
- Improved performance (approximately 20%) of the time integration and nonlinear solver libraries via modified solver defaults and enhanced step-control heuristics.
- Support for the Apple OS X operating systems (serial) in addition to the large number of supported platforms.
- A new default parser that provides for much improved detection of netlist errors and warnings.
- Added "-v" command line option that will report the current version number being run.
- Support for initial conditions on capacitors and inductors using the "IC = <value>" syntax will force the specified voltage drop at the beginning of a transient calculation.
- Support for new linear-solver controls (please see the updated **Xyce** Parallel Electronic Simulator User's Guide Version 1.1)
- Support for ChileSPICE-compatible voltage- and current-controlled sources in that the user may now specify a "VALUE={expression}" instead of being limited to linear coefficients.
- Support for netlist inline comments.

Specific Features and Enhancements

Here we give the list of new supported features and enhancements for **Xyce**. For details of each of these options statements, see the **Xyce**™ User's Guide.

New Device Support

- Radiation-aware (prompt-photo current) diode and BJT models.
- Support for PDE-devices that may be coupled with a larger analog circuit.
- Implemented "ON" and "OFF" instance specifications in the voltage controlled switch in a SPICE-compatible way.

The complete device list is given in the table below:

Device	Comments
Resistor	Semiconductor
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductance (see below)
Diode (Level 1)	
Diode (Level 3) – radiation aware	Prompt photocurrent radiation model.
VCVS (voltage controlled voltage source)	ChileSPICE compatible
VCCS (voltage controlled current source)	ChileSPICE compatible
VSRC (independent voltage source)	
ISRC (independent current source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2) – radiation aware	Prompt photocurrent radiation model.
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (BSIM3)	
Voltage-controlled switch (VSWITCH)	
Nonlinear Mutual Inductor	Sandia core model (not fully PSpice compatible)
Lossless Transmission Line	
BSRC (behavioral modeling source)	
PDE Devices	Both 1D and 2D drift-diffusion models of semiconductor devices are available, though not officially supported. Official support for these devices will accompany a future release.

Robustness Improvements

- New time-integration and nonlinear-solver heuristics as well as default tolerances that provide improved robustness.

Performance Improvements

Performance enhancements in this release account for an approximately 20% speed improvement for serial computations. The specific improvements include:

- Improved performance of the default serial sparse-direct linear solver (KSparse) of approximately 30%.
- Direct-access matrices are now on by default as are direct-access vectors for load calculations.
- Other miscellaneous internal code optimizations.

Interface Improvements

- XML metadata-based parser that allows for better integration with external tools by providing a common source for device data and parameters. It also provides much better error trapping.

Platform Support

- Support for Apple's OS X operating system (serial) in addition to the large number of supported platforms.

Miscellaneous

- Automated testing using a newly developed framework (Xyce Testing Framework – XTF) that facilitates various types of tests across multiple platforms.

Defects Fixed in this Release

Please note that these are the defects which might have possibly been encountered by the users of the code. There were many addition defects fixed but these were transparent to the end users.

Defect	Description
BSOURCE does not support for MAX & MIN	**Xyce** was returning 0 (zero) instead of evaluating the expressions.
When running in parallel, **Xyce** would hang on error or warning messages.	The parser was not handling the error reporting properly for parallel runs – now it does.

Defect	Description
Subcircuit calls were interfering with parsing of the next line.	When a subcircuit instance is expanded, the context for that subcircuit (i.e. the subcircuit definition) must be located. The process of doing this was losing the previous context, which has to be restored after the particular instance has completed expansion. The fix makes sure the previous context is properly saved for later restoration.
Change photocurrent scaling factor from instance "AREA" parameter to something else.	As initially received, the radiation aware BJT and diode used the instance-line "AREA" parameter to scale the photocurrent. Added a "DEVICEAREA" model parameter that is to be used *solely* as the area in photocurrent expressions.
Bug in atanh expression function.	Bounds checking on the function was incorrect and has now been fixed.
In the User's Guide, the resistor netlist reference shows invalid examples.	The netlist reference pages for the resistor device shows the following example: RLOAD 3 6 4.540 TC=.01,-.001 This syntax is not recognized by **Xyce**. The TC=a,b is achievable by a workaround using model statements.
The expression library is not handling nested functions in B-sources correctly.	If a B-source contained nested functions such as: B1 n1 n2 V={f(g(val))} then the function g did not get resolved properly. Now it does.
Memory leak in the expression library.	Fixed by removal of incorrectly deleted c-style arrays and replacement with std::vector's.
Indexing problems for parallel runs with BSRC device.	Incorrect Indexing of dependent solution variable lookup for expressions in the BSRC device due to use of GID rather than LID for indexing. Fixed.

Known Defects and Workarounds

Defect	Description
DC Sweep output.	DC sweep calculation does not automatically output sweep results *Workaround:* Use .PRINT statement to output sweep variable results.
Failure for netlists using ChileSPICE digital primitives.	**Xyce** does not currently support the use of digital primitives.
Xyce will not accept string parameters in models.	*Workaround:* Use integer for these values instead.

Defect	Description
Failures for parallel runs of small circuits. Often exhibits an "assert" error in the EDT_CrsGraph_View object.	This problem is usually encountered for relatively small circuits (<10 devices) which should generally be run with serial versions of **Xyce**. *Workaround:* Run parallel **Xyce** with command line option –dma off or run problem with serial version of **Xyce**.
Model statements contained within subcircuits that have model parameters defined in terms of subcircuit parameters will not be defined correctly in all subcircuit instances.	*Workaround:* Specify all models uniquely without reference subcircuit parameters.
Subcircuit instances can have their default parameters improperly overridden and no longer accessible.	*Workaround:* Specify at least one parameter on the subcircuit instance line for any subcircuit defined with a parameter list.

Incompatibilities With Other Circuit Simulators

Issue	Comment
.SAVE does not work	**Xyce** does not support this. Use .PRINT instead.
.OP is incomplete	A .OP netlist will run in **Xyce**, but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero	A requested pulsed source rise/fall time of zero really is zero in **Xyce**. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand	Output variables have to be specified as V(node) or I(source). Just putting node alone will not work.
BSIM3 level	In **Xyce** the BSIM3 is level=9. Other simulators have different levels for the BSIM3.
Node names vs. device names	Currently, circuit nodes and devices MUST have different names in **Xyce**. Some simulators can handle a device and a node with the same name, but **Xyce** cannot.
Interactive mode	**Xyce** does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources"	These are not currently supported within **Xyce**. *However…* **Xyce** does support "IC=<value>" statements for capacitors and inductors which will automatically set these voltage drops at the beginning of a transient simulation.

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